**In the claims:**

1. (currently amended) A semiconductor device, comprising:

a logic circuit, which includes a pair of complementary serially connected MOS transistors coupled between a voltage supply source and a reference voltage source, the transistor coupled to said reference voltage source having a lower leakage and driving current than the other of said complementary serially connected MOS transistors, and

a bias voltage supply circuit ~~comprising no more than two transistors each having its gate coupled to receive a control signal the logical reverse of the control signal received by the other transistor,~~ which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the other of said complementary serially connected MOS transistors.

2. (original) The semiconductor device of Claim 1, wherein the bias voltage supply circuit includes a first MOS transistor connected between a first voltage supply line and a bias voltage supply line and a second MOS transistor connected between a second voltage supply line and the bias voltage supply line, and said first or second bias voltage is output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor.

3. (canceled)

4. (currently amended) The semiconductor device of Claim 3, wherein the other of said MOS transistors of the logic circuit is a PMOS transistor and the other transistor of said logic circuit is an NMOS transistor ~~first MOS transistor and second MOS transistor are PMOS transistors~~.

5. (canceled)

6. (currently amended) The semiconductor device of Claim 1, wherein ~~the first bias voltage is lower than the second bias voltage~~ one said bias voltage is above the threshold voltage of said other of said complementary serially connected MOS transistors and the other said bias voltage is below the threshold voltage of said other of said complementary serially connected MOS transistors.

C1 cont'd

7. (previously presented) The semiconductor device of Claim 1, further including at least one additional logic circuit coupled to the bias voltage supply circuit.

8. (currently amended) A semiconductor device, comprising:

a logic circuit comprising a first MOS transistor and a second MOS transistor connected in series between the supply line of a power supply voltage and ground potential, a substrate region of said second MOS transistor being permanently coupled to ground potential, the second transistor having a lower leakage and driving current than the other of said complementary serially connected MOS transistors; and

a bias voltage supply circuit which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the first MOS transistor~~, said bias voltage supply circuit comprising no more than two transistors each having its gate coupled to receive a control signal the logical reverse of the control signal received by the other transistor~~.

9. (previously presented) The semiconductor device of Claim 8, wherein the first MOS transistor is a PMOS transistor and the second MOS transistor is an NMOS transistor.

10. (previously presented) The semiconductor circuit of Claim 8, wherein the first bias voltage is lower than the second bias voltage.

11. (currently amended) ~~The semiconductor circuit of Claim 8, wherein the first MOS transistor has a lower threshold voltage than said second MOS transistor.~~ A semiconductor device, comprising:

C1 cont'd

a logic circuit comprising a first MOS transistor and a second MOS transistor connected in series between the supply line of a power supply voltage and ground potential, a substrate region of said second MOS transistor being permanently coupled to ground potential, the second transistor having a higher threshold voltage than said first MOS transistor, and

a bias voltage supply circuit which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the first MOS transistor.

12. (previously presented) The semiconductor circuit of Claim 8, wherein the first bias voltage is lower than the second bias voltage.

13. (previously presented) The semiconductor circuit of Claim 8, wherein the bias voltage supply circuit includes a first MOS transistor connected between a first voltage supply line and a bias voltage supply line and a second MOS transistor connected between a second voltage supply line and the bias voltage supply line, and said first or second bias voltage is output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor.

Cl cont'd

14. (previously presented) The semiconductor circuit of Claim 13, wherein the MOS transistor of the logic circuit is connected to the first voltage supply line.

15. (previously presented) The semiconductor circuit of Claim 14, wherein the MOS transistor of the logic circuit and the first MOS transistor and second MOS transistor are PMOS transistors.

16. (previously presented) The semiconductor circuit of Claim 15, wherein the logic circuit includes an NMOS transistor connected between the PMOS transistor and a third voltage supply line.

17. (currently amended) A semiconductor device, comprising:

a logic circuit comprising a first MOS transistor and a second MOS transistor connected in series between the supply line of a power supply voltage and ground potential, the second transistor having a lower leakage and driving current than the other of said complementary serially connected MOS transistors;

a first bias voltage supply circuit~~, comprising no more than two transistors each having its gate coupled to receive a control signal the logical reverse of the control signal received by the other transistor,~~ which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the first MOS transistor; and

C1 cont'd

a second bias voltage supply circuit~~, comprising no more than two transistors each having its gate coupled to receive a control signal the logical reverse of the control signal received by the other transistor,~~ which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the second MOS transistor.

18. (previously presented) The semiconductor device of Claim 17, wherein the first MOS transistor is a PMOS transistor and the second MOS transistor is an NMOS transistor.

19. (previously presented) The semiconductor circuit of Claim 17, wherein the first bias voltage from the first bias supply circuit is lower than the second bias voltage from the first bias supply circuit.

20. (previously presented) The semiconductor circuit of Claim 17, wherein the first bias voltage from the second bias supply circuit is lower than the second bias voltage from the second bias supply circuit.

21. (previously presented) The semiconductor circuit of Claim 17, wherein the first MOS transistor has a lower threshold voltage than said second MOS transistor.

22. (previously presented) The semiconductor circuit of Claim 17, wherein the first bias voltage supply circuit includes a first MOS transistor connected between a first voltage supply line and a bias voltage supply line and a second MOS transistor connected between a second voltage supply line and the bias voltage supply line, and said first or second bias voltage is output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor.

C1 cont'd

23. (previously presented) The semiconductor circuit of Claim 17, wherein the second bias voltage supply circuit includes a third MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and ground potential and a fourth MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and a first bias supply line.

24. (previously presented) The semiconductor circuit of Claim 17, wherein:

the first bias voltage supply circuit includes a first MOS transistor connected between a first voltage supply line and a bias voltage supply line and a second MOS transistor connected between a second voltage supply line and the bias voltage supply line, and said first or second bias voltage is output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor; and

the second bias voltage supply circuit includes a third MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and ground potential and a fourth MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and a third bias supply line.

C1 cont'd

25. (previously presented) The semiconductor circuit of Claim 22, wherein the first and second MOS transistors of the first bias voltage supply circuit are PMOS transistors.

26. (previously presented) The semiconductor circuit of Claim 23, wherein the first and second MOS transistors of the second bias voltage supply circuit are NMOS transistors.

27. (previously presented) The semiconductor circuit of Claim 22, wherein the first and second MOS transistors of the first bias voltage supply circuit are PMOS transistors and the first and second MOS transistors of the second bias voltage supply circuit are NMOS transistors.

Cl cont'd

28. (new) The semiconductor device of claim 11 wherein one of said bias voltages is above the threshold voltage of said first MOS transistor and the other of said bias voltages is below the threshold voltage of said first MOS transistor.